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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/724,839	Applicant(s) SCHUBERT ET AL.	
	Examiner Yolanda Wilson	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-17 and 25-28* is/are allowed.

6)☒ Claim(s) *18-24,29,32,35,36,40,46,49,52,53 and 57* is/are rejected.

7)☒ Claim(s) *30,31,33,34,37-39,41-45,47,48,50,51,54-56 and 58-62* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-17,25-28 are allowed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 18-22,24,29,32,36,40,46,49,53,57 are rejected under 35 U.S.C. 102(b) as being anticipated by Dervisoglu. As per claim 18, Dervisoglu discloses a trigger processing means for monitoring trigger events and issuing a trigger action based on one or more of the monitored trigger events in section 4.1.1 on page 6, "Logic analyzer Trigger circuit (LAT):..." Dervisoglu discloses at least one probe circuit means for patching at least one signal of the electronic circuit within the integrated circuit hardware product in section 4.1.1 on page 6, "Logic Analyzer Probes (LAP)..." Dervisoglu discloses said communication means for providing external access to said electronic monitoring circuit by the debugger system in section 4.1.1 on page 8, "The Logic Analyzer Interface circuit may rely on existing capability to execute serial scan operations in order to configure the LAP and LAT circuits as well as to empty the contents of the LAM after data has been captured in it."

4. As per claim 19, Dervisoglu discloses configuration means for storing configuration information for use in configuring said trigger processing means or said at least one probe means in section 4.1.1 on page 7, "Said multiplexing circuits use dedicated flip-flops to control their operations so that scan operations are used to configure (i.e. program) the LAPs as desired."

5. As per claim 20, Dervisoglu discloses a communication means provides external access to said configuration means in section 4.1.1 on page 8, "The Logic Analyzer Interface circuit may rely on existing capability to execute serial scan operations in order to configure the LAP and LAT circuits as well as to empty the contents of the LAM after data has been captured in it."

6. As per claim 21, Dervisoglu discloses a status register means for storing status information pertaining to the electronic circuit design in section 4.1.1 on page 8, "In one mode of operation the LAM [Logic Analyzer Memory] can function as a circular buffer such that data is captured continuously until the trigger condition has been met and a pre-defined number of cycles have elapsed."

7. As per claim 22, Dervisoglu discloses said communication means provides external access to said status register means in section 4.1.1 on page 8, "The Logic Analyzer Interface circuit may rely on existing capability to execute serial scan operations in order to configure the LAP and LAT circuits as well as to empty the contents of the LAM after data has been captured.

8. As per claim 24, Dervisoglu discloses the monitored trigger event include current trigger events and previous trigger events in section 4.1.1 on page 6, "Logic analyzer Trigger circuit (LAT)..."

9. As per claim 29, Dervisoglu discloses monitoring circuitry within an integrated circuit said monitoring circuitry to assist a debugger system in debugging an electronic circuit implemented within said integrated circuit, said electronic circuit comprising a finite state machine said finite state machine comprising combinatorial logic coupled between an output of a register and an input of said register in the abstract and section 4.1.1 on page 6, "Logic Analyzer Probes (LAP)".

Dervisoglu discloses said monitoring circuitry comprising: a) a communication link to communicate with said debugger system; b) a trigger processing unit to provide a trigger signal if said finite state machine reaches a looked for state, said trigger processing unit comprising a trigger register and comparison circuitry, said trigger register to be set by said debugger system through said communication link to define said looked for state, said comparison circuitry having a first input coupled to an output of said trigger register and a second input coupled to said output of said register, said comparison circuitry to generate said trigger signal; and c) sample circuitry inserted into said electronic circuit, said sample circuitry coupled to said trigger processing unit said sample circuitry to sample a signal within said electronic circuit in response to said trigger signal on pages 6 - 7, section 4.1.1.

10. As per claim 32, Dervisoglu discloses said finite state machine is a one hot encoded finite state machine and said trigger register is set by setting a single bit in said

trigger register to a logical "1" on page 7, "At it core, the LAT is a programmable circuit that used scan controller flip-flops to select among Boolean terms and higher-level signal values."

11. As per claim 36, Dervisoglu discloses monitoring circuitry within an integrated circuit said monitoring circuitry to assist a debugger system in debugging an electronic circuit implemented within said integrated circuit, said electronic circuit comprising a finite state machine said finite state machine comprising combinatorial logic coupled between an output of a register and an input of said register in the abstract and section 4.1.1 on page 6, "Logic Analyzer Probes (LAP)".

Dervisoglu discloses said monitoring circuitry comprising: a) a communication link to communicate with said debugger system; b) a trigger processing unit to provide a trigger signal if said finite state machine reaches a looked for state, said trigger processing unit comprising a trigger register and comparison circuitry, said trigger register to be set by said debugger system through said communication link to define said looked for state, said comparison circuitry having a first input coupled to an output of said trigger register and a second input coupled to both said finite state machine's combinatorial logic and said output of said register, said comparison circuitry to generate said trigger signal; and c) sample circuitry inserted into said electronic circuit, said sample circuitry coupled to said trigger processing unit said sample circuitry to sample a signal within said electronic circuit in response to said trigger signal on pages 6 - 7, section 4.1.1.

12. As per claim 40, Dervisoglu discloses said finite state machine is a one hot encoded finite state machine and said trigger register is set by setting a single bit in said trigger register to a logical "1" on page 7, "At it core, the LAT is a programmable circuit that used scan controller flip-flops to select among Boolean terms and higher-level signal values."

13. As per claim 46, Dervisoglu discloses monitoring circuitry within an electronic system said electronic system comprising electronic components, said monitoring circuitry to assist a debugger system in debugging an electronic circuit implemented within said integrated circuit, said electronic circuit comprising a finite state machine said finite state machine comprising combinatorial logic coupled between an output of a register and an input of said register in the abstract and section 4.1.1 on page 6, "Logic Analyzer Probes (LAP)".

Dervisoglu discloses said monitoring circuitry comprising: a) a communication link to communicate with said debugger system; b) a trigger processing unit to provide a trigger signal if said finite state machine reaches a looked for state, said trigger processing unit comprising a trigger register and comparison circuitry, said trigger register to be set by said debugger system through said communication link to define said looked for state, said comparison circuitry having a first input coupled to an output of said trigger register and a second input coupled to said output of said register, said comparison circuitry to generate said trigger signal; and c) sample circuitry inserted into said electronic circuit, said sample circuitry coupled to said trigger processing unit said

sample circuitry to sample a signal within said electronic circuit in response to said trigger signal on pages 6 - 7, section 4.1.1.

14. As per claim 49, Dervisoglu discloses said finite state machine is a one hot encoded finite state machine and said trigger register is set by setting a single bit in said trigger register to a logical "1" on page 7, "At it core, the LAT is a programmable circuit that used scan controller flip-flops to select among Boolean terms and higher-level signal values."

15. As per claim 53, Dervisoglu discloses monitoring circuitry within an electronic system comprising electronic components, said monitoring circuitry to assist a debugger system in debugging an electronic circuit implemented within said integrated circuit, said electronic circuit comprising a finite state machine said finite state machine comprising combinatorial logic coupled between an output of a register and an input of said register in the abstract and section 4.1.1 on page 6, "Logic Analyzer Probes (LAP)".

Dervisoglu discloses said monitoring circuitry comprising: a) a communication link to communicate with said debugger system; b) a trigger processing unit to provide a trigger signal if said finite state machine reaches a looked for state, said trigger processing unit comprising a trigger register and comparison circuitry, said trigger register to be set by said debugger system through said communication link to define said looked for state, said comparison circuitry having a first input coupled to an output of said trigger register and a second input coupled to both said finite state machine's combinatorial logic and said output of said register, said comparison circuitry to generate said trigger signal; and c) sample circuitry inserted into said electronic circuit,

said sample circuitry coupled to said trigger processing unit said sample circuitry to sample a signal within said electronic circuit in response to said trigger signal on pages 6 - 7, section 4.1.1.

16. As per claim 57, Dervisoglu discloses said finite state machine is a one hot encoded finite state machine and said trigger register is set by setting a single bit in said trigger register to a logical "1" on page 7, "At it core, the LAT is a programmable circuit that used scan controller flip-flops to select among Boolean terms and higher-level signal values."

17. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dervisoglu in view of Whetsel (USPN 6378093B1). As appears in claims 4,13,23, Dervisoglu fails to explicitly state an analog-to-digital converter coupled between said at least one probe circuit and the electronic circuit design within the integrated circuit hardware product to provide analog-to-digital conversion.

Whetsel discloses in column 29, lines 55-59, "...an integrated circuit 2350 includes an analog to digital converter (ADC) 2352 connected, in test mode, to a scan collector circuit 2354 at its digital output and to an integrated circuit pad or core terminal 2356 at its analog input."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have an analog-to-digital converter coupled between said at least one probe circuit and the electronic circuit design. A person of ordinary skill in the art would have been motivated to have an analog-to-digital converter coupled between said at least one probe circuit and the electronic circuit design because an

analog-to-digital converter is useful in converting signals from analog to digital whenever a circuit has analog signals and digital signals that need to be converted for processing.

18. Claims 35,52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dervisoglu in view of Kawamura et al. (USPN US005801956A). As appears in claims 8,15, Dervisoglu fails to explicitly said electronic monitoring circuit is derived from a HDL description of the electronic circuit design.

Kawamura et al. discloses in column 1, lines 26-28, "HDL enables the direct description of detailed timing information and logic synthesis and operation verification can be conducted easily."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have an electronic monitoring circuit being derived from a HDL description of the electronic circuit design. A person of ordinary skill in the art would have been motivated to have an electronic monitoring circuit being derived from a HDL description of the electronic circuit design because HDL is a well known language that is used in the designing of integrated circuits. Kawamura et al. discloses in column 1, lines 20-24, "Since it is necessary in such integrated circuits to design a logic circuit with gates numbering more than five hundred thousand, the current mainstream practice is to perform design by using the HDL."

Response to Arguments

19. Applicant's arguments with respect to claims 18-24, 29, 32, 35, 36, 40, 46, 49, 52, 53, 57 have been considered but are moot in view of the new ground(s) of rejection.

The amending of claim 18 and the addition of the new claims required a new grounds of rejection. With respect to claim 18, Dervisoglu does discloses patching, which is represented by the trigger circuit and its functions. With respect to the independent claims represented in claim 29-62, there is disclosed a finite state machine as indicated in the rejection of the claims above.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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